This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TPEL.2018.2830401, IEEE Transactions on Power Electronics

Switched-Capacitor Based Single Source Cascaded H-bridge Multilevel Inverter Featuring Boosting Ability

Hossein Khoun Jahan, Mehdi Abapour, Kazem Zare

Abstract-cascaded multilevel inverter (CMI) is one of the most popular multilevel inverter topologies. This topology is synthesized with some series connected identical H-bridge cells. CMI requires several isolated dc sources which brings about some difficulties when dealing with this type of inverter. This paper addresses the problem by proposing a switched capacitor (SC) based CMI. The proposed topology, which is referred to as switched capacitor single source CMI (SCSS-CMI), makes use of some capacitors instead of the dc sources. Hence it requires only one dc source to charge the employed capacitors. Usually, the capacitor charging process in a SC cell is companied by some current spikes which extremely harm the charging switch and the capacitor. The capacitors in SCSS-CMI are charged through a simple auxiliary circuit which eradicates the mentioned current spikes and provides zero current switching condition for the charging switch. A computer-aid simulated model along with a laboratory-built prototype are adopted to assess the performances of SCSS-CMI, under different conditions.

Index Terms—multilevel inverter, CMI, switched capacitor.

NOMENCLATURE

I_m	Maximum value of load current
f	Frequency of the output voltage
ω	$2\pi f$
θ	Load current angle
ℓ	Number of levels
v_{dc}	Voltage value of dc source
$v_{os_{cs}}$	On-state voltage of the charging switch
$v_{os_{cd}}$	On-state voltage of a charging diode
$v_{o_{fd}}$	On-state voltage of the freewheeling diode
t_m	Starting instance of the mth level at the first quarter of a cycle
t_{b+n}	Starting instance of the (b+n)th level at the second quarter of a cycle
T_n	Time duration of the nth level
Du_n	Time duration in which the nth capacitor takes part in developing a voltage level
v_{c_1}	Voltage of the capacitor participating in the first level
Δv_{c1}	Highest voltage drop in a capacitor (C_1)
$v_k(t)$	Voltage in kth H-Bridge cell
$v_k(0)$	Initial voltage of the capacitor in the kth H-bride cell at the starting instance of a cycle
$v_k(\pi/\omega)$	Initial voltage of the capacitor in the kth H-bride cell at the end of a half cycle
Δv_k	Highest voltage variation of the capacitor in the kth H-bride cell
R	Load resistance
C_k	Capacitance of capacitor in the kth H-bridge cell
T_{ch}	Charging time duration
ω_{ch}	$2\pi/T_{ch}$
R_{cs}	Resistance of the charging switch
$R_{d_{ch}}$	Resistance of a the charging diode
R_{d_f}	Resistance of the freewheeling diode
R_l	Resistance of the charging inductor
i_{ch}	Charging current
L_{ch}	Inductance of the charging inductor
P_{loss}^{FCS}	Total power loss of the charging stage in the presence of the first charging structure
P_{loss}^{SCS}	Total power loss of the charging stage in the presence of the second charging structure

I. INTRODUCTION

Multilevel inverters are one of the state-of-the-art constituents in modern electrical power systems. They take part in many applications such as renewable energy systems, machine drives, electrical vehicles, and etc. [1-3]. The main advantages related to them are: i) realizing voltage of lower total harmonic distortion (THD), ii) requiring components of lower voltage stress, and iii) Mitigating electromagnetic interference (EMI). On the contrary, requiring extra number of components is the fatal demerit of these kinds of converters [4]. However, to the end of lessening the mentioned drawback several topologies are introduced so far [5-7].

Diode-clamped converter (DCC), Flying-capacitor converter (FCC), and Cascaded multilevel inverter (CMI), are the most well know topologies of multilevel inverter [8-10]. Among these three topologies CMI stands out for its modular structure which makes it easy to be designed, synthesized, and repaired. However, this topology does suffer from requiring several isolated dc sources. This issue, apart from bringing about some physical problems like increasing cost and volume, arises some fatal difficulties to appear in its different applications. Hence, addressing this problem is of particular importance. However, some researchers have taken the advantage of needing some isolated dc sources to adopt CMI in photovoltaic (PV) applications [1][11]. As shown in these papers employing this inverter in PV applications calls for some individual dc-dc converters and an elaborate controlling system. Furthermore, CMI is considered to be workable in STATCOM application. In this application the dc sources are replaced with some capacitors [12-13]. Same as the PV application, CMI in STATCOM application requires a versatile controlling system to balance the voltage of the capacitors. We also encounter to some researches that attempt to reduce the number of dc sources in CMI. One solution is using low frequency transformers instead of several dc source [14-15]. Using transformers in CMI structure has its own pros and cons. By choosing proper transformer ratio, transformers can offer an arbitrary voltage value from a given input voltage value, they provide a galvanic isolation as well. On the contrary, they are bulky, expensive, and wasteful. The other solution is using a high frequency link and transform-

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TPEL.2018.2830401, IEEE Transactions on Power Electronics

er to provide several dc sources [16-17]. Although using a high frequency link and transformer reduces the total size, it calls for extra number of components to develop the high frequency link and several isolated dc sources.

Motivated by the issue, and to the end of reducing the dc sources in CMI, the present paper proposes a single-source switched capacitor based symmetric CMI. The suggested topology has some remarkable features. Firstly, it possesses a self-balancing capability. Secondly, it requires solely one dc source, the rest dc sources are replaced by some capacitors. The last but not least is its ability to offer a boosted staircase ac voltage. Consequently, regarding the mentioned features, the proposed topology can be a versatile converter in the industrial applications. For instants, by eradicating the leakage current and boosting the input voltage, SCSS-CMI can make the transformer needless in grid-tied PV application. In the present paper, two different charging structures are suggested to charge the capacitors in the main part of SCSS-CMI.

This paper is arranged as follows: in the next section the structure and operation principle of SCSS-CMI are explained. In section III, the proposed charging units are described. In section IV the capacitors voltage in the proposed topology are analyzed. In section V, by using a simulated model, which is simulated under Matlab/Simulink environment, the performance of SCSS-CMI is investigated. In order to lend credence to the feasibility of SCSS-CMI it is also tested by employing a laboratory-built prototype. The experimental results are provided in section VI. Finally, the overall work is concluded in section VII.

II. SCSS-CMI Configuration And Operation Principle

Generally, SCSS-CMI is composed of two different parts, namely the main and the charging (charging unit) parts. The main part is an arbitrary configuration of the conventional CMI which provides the load with a staircase ac voltage. The charging unit is synthesized with a dc source, charging inductor (L_{ch}), charging switch (S_{ch}), some charging diodes (D_n) and, a freewheeling diode (D_f). By using L_{ch}, the charging unit charges the capacitors with a smooth current. This unit is fully described in section III. Two different structures are proposed for the charging unit that each one has its own pros and cons. These structures are referred to as the first and the second charging structures.

These structures, which are fully described in the forthcoming subsections, can be used in a symmetric CMI with an arbitrary number of H-bridge cells, however for the sake of simplicity a nine-level CMI (four-cell configuration) is considered to be equipped with the mentioned charging structures. It is worth mentioning that, in the forthcoming subsections the states of the components are described in some tables, in these tables "*0*" and "*1*" are, respectively, indicative of "*on*" and "*off*" states of the switches and diodes. All the capacitors in SCSS-CMI experience three different modes which are referred to as charging, discharging, and disconnecting modes. In the tables 'C', 'D', and 'N' demonstrate the charging, discharging, and disconnecting modes of the capacitors, respectively. It should also be noted that, since all the lower switches in the main part have complementary states with the upper switches, their states are not cited in the tables. For the sake of clarity, in the SCSS-CMI configurations, which are shown in the forthcoming subsections, the main part (the conventional CMI) is shown in black color while the charging structures are in blue.

A. first charging structure

Fig. 1 shows a nine-level SCSS-CMI which employs the first charging structure, and Table I tabulates the states of the components and the switching patterns of the voltage levels in this configuration. As depicted, the main part in the suggested topology is synthesized with some identical H-bridge cells. Therefore, alike the conventional CMI, the modularity in SCSS-CMI is preserved. As shown, a SCSS-CMI equipped with the first charging structure offers a common ground which is shared by the ac and dc sides. This is very advantageous feature in photovoltaic and ac-dc hybrid micro grid applications, as they require a common ground for the ac and dc sides. Especially, in the photovoltaic systems this feature could eradicate the problem of leakage current which is one of the most troublesome issues in these systems [18]. On the contrary, as it is discernable in Table I, the most bothersome characteristic of this structure is its inability to provide a continuous power flow. This can be counted as a negligible problem in the micro grid applications if the dc micro grid is considered huge enough to digest the harmonics which appear due to the discrete current drawn by this inverter. Nevertheless, this is not the case in the photovoltaic application and the non-continuous input current can cause some difficulties, thus some measures should be resorted to address this problem in the mentioned application. It is worth mentioning that, the problem of non-continuous input current exists in the virtual dc bus based invert [19-20], and charge pump based inverter [18] which are some well-known or new topologies in the grid-tied PV application. However, since these inverters along with SCSS-CMI, eradicate the need for the bulky and expensive transformer in the grid-tied PV system, employing some ancillary devices to address the mentioned problem in these topologies is justified. It is worth mentioning that, this problem does not appear in a three-phase configuration of SCSS-CMI.

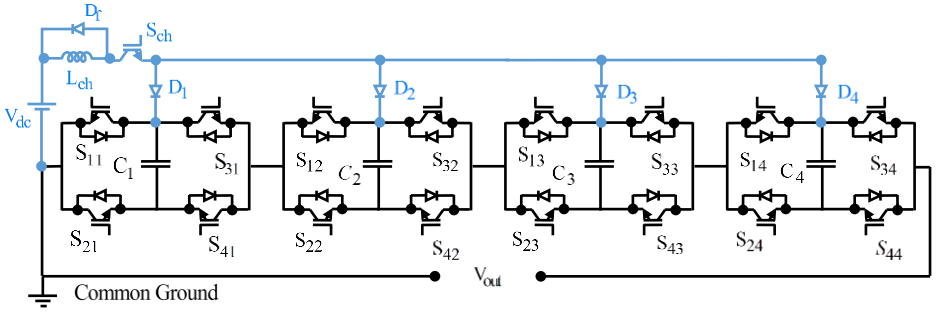


Fig. 1. Nine-level SCSS-CMI with the first charging structure

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TPEL.2018.2830401, IEEE Transactions on Power Electronics

TABLE I
OPERATION STATES OF COMPONENTS IN THE FIRST CHARGING STRUCTURE

levels	main switches	Charging switch	Charging Diodes	Capacitors
	$S_{11},S_{31},S_{12},S_{32}$ $S_{13},S_{33},S_{14},S_{34}$	S_{ch}	$D_1,D_2,$ $D_3.D_4$	C_1,C_2,C_3,C_4
4	01010101	1	1000	C,D,D,D
3	00010101	1	1100	C,C,D,D
2	00000101	1	1110	C,C,C,D
1	00000001	1	1111	C,C,C,C
0	00000000	1	1111	C,C,C,C
-1	10000000	0	0000	D,N,NN
-2	10100000	0	0000	D,D,N,N
-3	10101000	0	0000	D,D,D,N
-4	10101010	0	0000	D,D,D,D

B. *Second charging structure*

As discussed earlier the main drawback of the first structure is its inability to provide a continuous power flow at the input side. This problem can be addressed by relocating the dc source in each half cycle. As depicted in Fig. 2 and shown in Table II, the dc source is relocated through two charging switches (S_{Lch} and S_{Rch}). This structure loses the common ground for the ac and dc sides. Featuring the ability to provide a continuous power flow at the input side makes this structure suitable for PV and battery applications.

As it is mentioned in [21], if a CMI is used in a grid-tied PV application, there appear some bothersome leakage currents between the PV cells inserted in the H-bridge cells. To eradicate these leakage currents in such an application, a complex filter configuration is needed. The procedure of the filter design for the mentioned system is meticulously explained in [21]. Nonetheless, since the SCSS-CMI with the second charging structure needs only one dc-source (the dc-source could be a PV string) this topology needs a simple filter to eliminate the mentioned leakage current. However because this issue is out of the scope of this paper we refrain from investigation it.

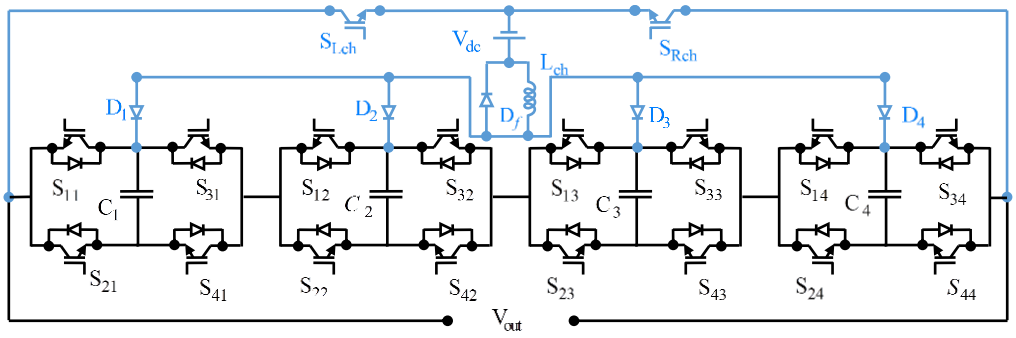


Fig. 2. Nine-level SCSS-CMI with the second charging structure

TABLE II
OPERATION STATES OF COMPONENTS IN THE SECOND CHARGING STRUCTURE

levels	Main switches	Charging switches	Diodes	Capacitors
	$S_{11},S_{31},S_{12},S_{32}$ $S_{13},S_{33},S_{14},S_{34}$	S_{Lch}, S_{Rch}	$D_1,D_2,$ $D_3.D_4$	C_1,C_2,C_3,C_4
4	01010101	10	1000	C,D,D,D
3	00010101	10	1100	C,C,D,D
2	00000101	10	1110	C,C,C,D
1	00000001	10	1111	C,C,C,C
0	00000000	11	1111	C,C,C,C
-1	10000000	01	1111	C,C,C,C
-2	10100000	01	0111	D,C,C,C
-3	10101000	01	0011	D,D,C,C
-4	10101010	01	0001	D,D,D,C

C. *Three-phase SCSS-CMI*

In the three-phase applications the charging unit must be connected to the neutral point, So the suitable structure for a three-phase SCSS-CMI is employing the first charging structure, so that, there would be no need for three individual charging units. In order to bring more clarity to the issue, a typical three-phase SCSS-CMI is depicted in Fig. 3. It is interesting to be mentioned that, as asserted earlier, in SCSS-CMI the dc source only joins to the circuit in some switching intervals to charge the capacitors, this implies that it does not directly provide a path for the load current. This feature can be taken into consideration to design a workable protection plat to protect the components and the dc source in faulty conditions.

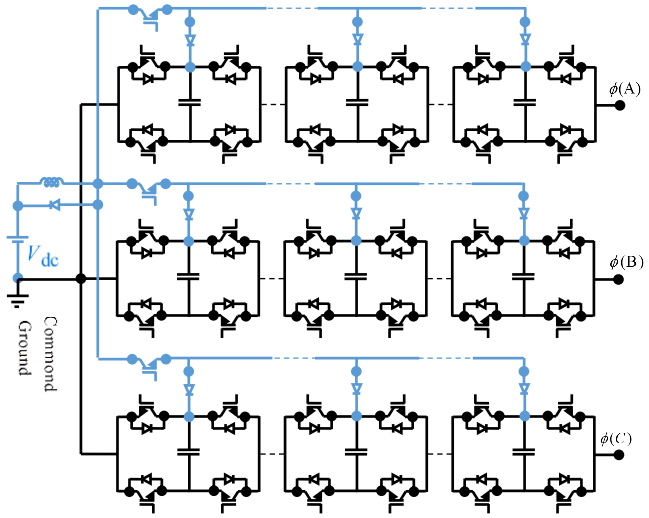


Fig. 3. Typical three-phase configuration of SCSS-CMI.

D. *Evaluation of the charging structures*

As defined earlier, each of the proposed charging structures has some especial features. In order to provide a brief overview and evaluate the suggested charging structures, their features are juxtaposed in Table III. In this table ϕ is indicative of phase. It is to be noted that, since these structures have the same conventional CMI as their main parts, the components required to synthesize the main parts are not listed in Table III. However we can add $2(\ell-1)$ number of switches and $(\ell-1)/2$ number of capacitors to the presented list as the components required to construct the main part in these structures.

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TPEL.2018.2830401, IEEE Transactions on Power Electronics

TABLE III
OVERVIEW OF THE SUGGESTED CHARGING STRUCTURES

Charging structure	Charging switch		Charging diode		Freewheeling diode	Three-phase (3ϕ) possibility	Continuous Input Power flow		Ability to offer a common ground
	Count	Maximum Forward blocking voltage	Count	Peak Invers voltage			3ϕ	1ϕ	
First	1	$(\ell-3)V_{dc}/2$	$(\ell-1)/2$	(n-1)v_{dc}	1	Yes	Yes	No	Yes
Second	2	$(\ell-3)V_{dc}/2$	$(\ell-1)/2$	(n-1)v_{dc}	1	No	-	Yes	No

III. CAPACITORS CHARGING UNIT

The capacitors charging process is of great importance in the SC based converters. Charging of capacitors in these kinds of converters brings about some successive inrush currents which are harmful for the capacitors, charging switch, and the dc source. Although these inrush currents are, to some extent, mitigated by resistive characteristic of the charging current paths, these limitation are insignificant and wasteful. Usually the attempt is exerted to reduce the mentioned resistive characteristics of the current path to mitigate power loss. Therefore, solving this problem seems to be of crucial importance. To overcome this constraint in SCSS-CMI an inductor is connected in series with the dc source and the charging switch. Obviously, the current interruption in an inductor causes a voltage spike which is a harmful phenomenon for the breaker switch. Therefore a measure should be resorted to avert this phenomenon. The first solution is to choose the inductance value of the charging inductor in a way that the charging switch acts under zero current condition. Since the charging period in the first charging structure lasts for a half cycle, to ensure zero current switching of the charging switch and properly mitigate the inrush current, the resonant frequency of the inductor and the equivalent capacitors must be equal to the output voltage frequency. Consequently, the smallest size for the charging inductor is figured out by equation (1).

The second and more reasonable solution for the mentioned problem is to connect a freewheeling diode in parallel with the inductor in a way that the diode provides a freewheeling path for the interrupted current. In this solution the charging inductor size can be chosen large enough to have a smoother current at the input side. Apart from avoiding the mentioned voltage spikes, the freewheeling diode can prevent the capacitors from overcharging. This is a very essential feature, because the overcharging phenomenon can cause the voltages of capacitors to reach to two times the nominal value, so the capacitor can be harshly damaged. To bring more clarity to the issue, let's consider the charging process of the capacitors in the first charging structure, this process is exhibited in Figs. 4(a) and (b), where Fig. 4(a) shows the charging process when the freewheeling diode is not present, and Fig. 4(b) depicts the same process in the presence of the freewheeling diode. In the mentioned figures the assumption is that the main part of SCSS-CMI is synthesized with 'α' number of ideal and identical H-bridge cells, also the size of the capacitors and charging inductor have been chosen in a way that the zero current switching condition is provided for the charging switch. According to Fig. 4(a), as voltage in the capacitors reaches to the input dc voltage value the current in the charging inductor reaches to its maximum value and lingers on until reaching to its zero value, this continuation brings about overvoltage to take place in the capacitors and harm them. However, as shown in Fig. 4(b), employing the freewheeling diode provides a detour path for the inductor current as the switch interrupts it, hence, the overvoltage is averted. Additionally, as mentioned earlier, the byproduct of employing such a diode is the facility of adopting a larger size for the charging inductor. Apart from smoothing the input current, a large charging inductor can be useful to limit the fault current and protect the components under any faulty condition. It is worth noting that, since in the second charging structure there is no input current interruption and a continuous current flows through the charging inductor, the freewheeling diode is not for averting the voltage spikes, but it is required to avoid the overcharging phenomenon. The freewheeling diode is a handy device for a fault tolerant plat as well. Usually the fault tolerant plats require some relays to isolate the faulty parts [22]. However, relays are slow and they require some complex circuits. The fault tolerant plat for the SCSS-CMI would not require extra device to protect the components if the charging switches are turned off when a fault occurs. However, if the freewheeling diode is not present, the current interruption can harshly damage these switches, because they are designed to function under zero current condition. It makes sense that if the freewheeling diode is adopted, the zero current condition is provided for the charging switches even in fault current interruption.

There may also be a suspicion that the inrush current may flow among the parallel capacitors due to differences in their charging state and parameters. However, as illustrated earlier, the capacitor can experience only three different states, namely charging, discharging, and disconnecting states. A capacitor in the disconnecting state does not participate in any activity, so there would not be any inrush current possibility in this state. In discharging state the capacitors connect to each other and the load in series, so they can only carry the load current, thus there is no way to the inrush current as well. Finally, as shown in Fig. 4(a) and (b), in the charging state, the charging capacitors are in parallel and are charged through the charging diodes. In this state the changing diodes block the charge exchanges between the capacitors, as the result, in this state, as well as the other two states, the inrush current is impossible.

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TPEL.2018.2830401, IEEE Transactions on Power Electronics

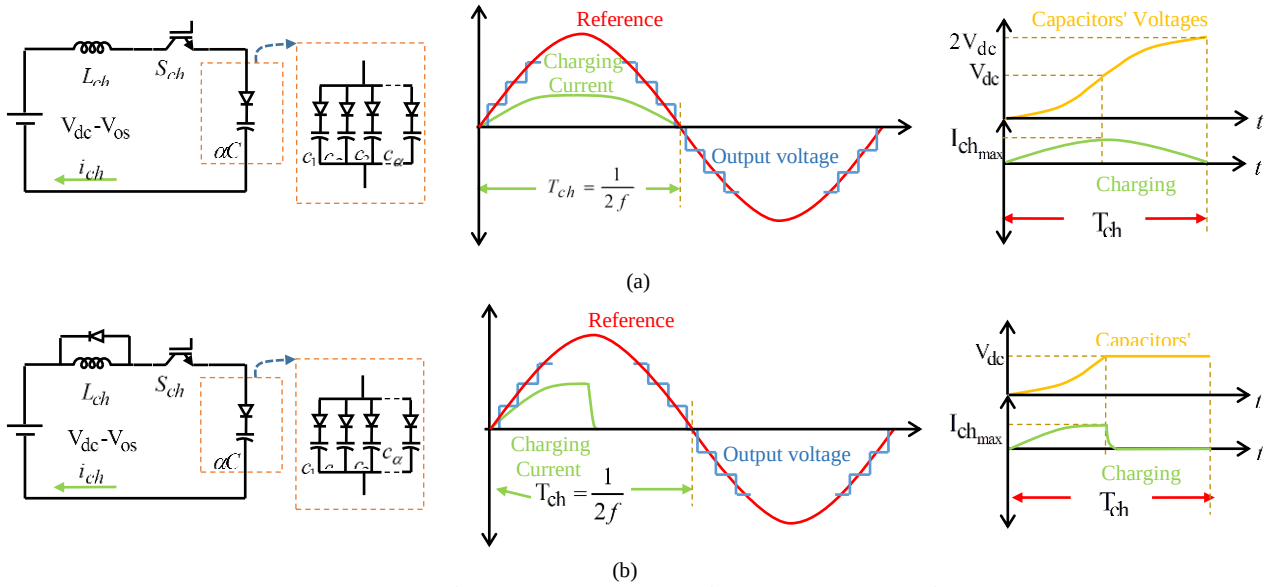


Fig. 4. Schematic diagram of charging mode. (a) Without freewheel-diode. (b) with freewheel diode

$$L_{ch} = \frac{1}{(2\pi f)^2 \alpha C} \tag{1}$$

Equation (2) describes the charging current and no-load voltage condition of the capacitors according to Fig. 4(a). Meanwhile, the charging current and no-load voltage condition of the capacitors, according to Fig. 4(b), are illustrated in equation (3).

$$\begin{cases} i_{ch}(t) = \dfrac{\Delta v}{L_{ch}\omega_{ch}} \sin \omega_{ch} t \\ v_c(t) = v_{dc} - L_{ch}\dfrac{di_{ch}}{dt} = v_{dc}\left(1 - \cos \omega_{ch} t\right) \\ \omega_{ch} = \dfrac{1}{\sqrt{\alpha C L_{ch}}} \\ 0 \le \omega_{ch} t \le \pi \end{cases} \tag{2}$$

$$\begin{cases} i_{ch}(t) = \dfrac{\Delta v}{L_{ch}\omega_{ch}} \sin \omega_{ch} t & 0 \le \omega_{ch} \le \dfrac{\pi}{2} \\ i_{ch}(t) = 0 & \dfrac{\pi}{2} \le \omega_{ch} t \le \pi \\ v_c(t) = v_{dc} - L_{ch}\dfrac{di_{ch}}{dt} = v_{dc} - \Delta v \cos \omega_{ch} t & 0 \le \omega_{ch} \le \dfrac{\pi}{2} \\ v_c(t) = v_{dc} & \dfrac{\pi}{2} \le \omega_{ch} t \le \pi \\ \omega_{ch} = \dfrac{1}{\sqrt{\alpha C L_{ch}}} \end{cases} \tag{3}$$

The total power loss of charging stage in the first, and second charging structures are, respectively, figured out by (4), and (5). It is worth mentioning that since S_{ch} turns *on* and *off* in zero current condition the switching power loss related to this switch is cancelled out in the charging stage.

$$P_{loss}^{FCS} = f\int_0^{\frac{1}{2f}} \left[(R_{cs} + R_l + R_{d_{ch}}) i_{ch}^2(t) + (v_{os_{cs}} + v_{os_{cd}}) i_{ch}(t)\right] dt + \frac{1}{2}\left((R_{d_f} + R_l) i_{ch}^2\left(\frac{1}{2f}\right) + v_{o_{fd}} i_{ch}\left(\frac{1}{2f}\right)\right) \tag{4}$$

$$P_{loss}^{SCS} = f\int_0^{\frac{1}{f}} \left[(R_{cs} + R_l + R_{d_{ch}}) i_{ch}^2(t) + (v_{os_{cs}} + v_{os_{cd}}) i_{ch}(t)\right] dt \tag{5}$$

Capacitor Voltage Analysis

Several factors like load power factor, amount of supplied power, frequency of the desired ac voltage, modulation methods, and etc. can affect voltage in a SC cell. So far, in literatures several modulation methods have been put forth for CMI [23-25]. However, because there is some limited pattern to develop some of the levels in SCSS-CMI, level-shifted sinusoidal pulse width modulation (LS-SPWM) strategy [26] is the most compatible strategy for this topology. Therefore this strategy is employed to investigate the capacitors voltage. For the sake of simplicity and to assume the worst voltage variation, the level-shifted triangular carriers in the mentioned strategy are replaced with some straight lines. The switching signals are computed by comparing the reference waveform with the considered straight lines, as shown in Fig 5. However there are several switching patterns to develop some of the voltage levels, the patterns in which the higher number of capacitors are in the charging states should be the patterns of chose. So that, the voltage drop in the capacitors would decrease. Additionally, a nine-level SCSS-CMI (SCSS-CMI with four H-bridge cells) is considered to work out a clear investigation.

Since in the first charging structure, for a rest of the negative half cycle all the capacitors provide the load current without being charged, the voltage drop in this structure would be higher than that in the second structure. On the other hand, respect to the other capacitors in this structure, C_1 provides the load current for a longer time, so it experiences the highest voltage drop. Hence, voltage of C_1 (v_{C_1}) in the first charging structure is taken into consideration to figure out the highest voltage drop. Also a pure resistance (R) is assumed as the load.

For a ℓ-level SCSS-CMI, the time duration of each level, in an half cycle, is shown in Fig. 5 and described by equations (6) to (8). Moreover, for the considered nine-level SCSS-CMI, the equivalent circuits for the voltage levels in a half cycle are depicted in Fig. 6 and the related output voltage are explained in (9) - (16). It goes without saying that, since in the zero level C_1 is in the charging mode, its voltage is equal to the input dc voltage. As shown in Fig.6 (b), in the first voltage level only C_1 con-

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TPEL.2018.2830401, IEEE Transactions on Power Electronics

nects to the load, so the time constant of the equivalent circuit is $1/RC$ and v_{C_1} is described by (10). At the end of this level output voltage becomes $v_o(t_1)$. Referring to Fig. 6 (c), in the second level C_2 connects to C_1 in series and the voltages in these two capacitors add up to develop the second voltage level (at the staring of this level v_{C_2} is equal to v_{dc} and v_{C_1} is equal to $v_o(t_1)$ so the initial value of the output voltage is $v_{dc}+v_o(t_1)$), also the time constant in this level becomes $(C_1+C_2)/RC_1C_2$. Since all the capacitor are identical, the time constant in the second level can also be presumed as $2/RC$. At the end of the second level the output voltage becomes $v_o(t_2)$. Accordingly, as shown in Fig. 6(d), (e), (f), (g), and (h) the same procedure can be considered for the other stages and levels. As depicted in Fig. 6(h), v_{C_1} reaches to its lowest value almost at the end the half cycle (before reaching level 0 at the end of the half cycle). Since the highest value of v_{C_1} is equal to the input dc voltage (v_{dc}), subtracting the voltage value obtained by (16) from v_{dc}, gives the highest voltage variation in C_1. Fig. 6(i) depicts voltage of each capacitor in different voltage-levels for a nine-level SCSS-CMI equipped with the first charging structure. Voltage drop in C_1 (the capacitor which participates in all the voltage levels and experiences the highest voltage drop) is approximated by (17), this parameter for different capacitors in an ℓ -level SCSS-CMI is approximated by (18). Fig. 7 visualizes the effects of the number of cells and output voltage frequency on the voltage drop in the capacitors. In this figure the load, capacitor capacitance and peak output voltage value are considered to be, pure resistive load of $10\,\Omega$, $4700\,\mu F$ and $220\sqrt{2}$ V ($2\times220\sqrt{2}/(\ell\text{-}1)$ V for each capacitor), respectively. Referring to Fig. 5, in a SCSS-CMI with a given power and voltage magnitude, the higher the number of cells (levels) or/and frequency of the output voltage are, the shorter the time duration of each level is. Also, shorter time duration for the levels implies lower discharging of the capacitors. Consequently, the lower discharging of capacitor causes lower voltage drop.

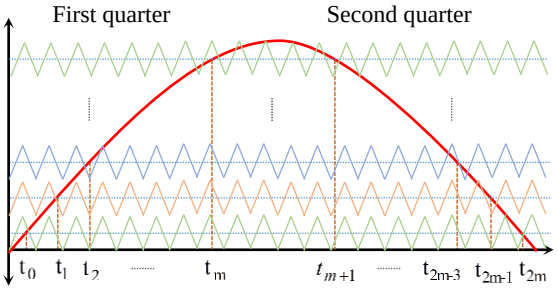


Fig. 5. Time duration of the levels.

$$t_m=\frac{1}{\omega}\sin^{-1}\left(\frac{1+2m}{\ell}\right) \quad (6)$$

$$t_{b+n}=\frac{1}{\omega}(\pi-t_{(b-n)}) \quad (7)$$

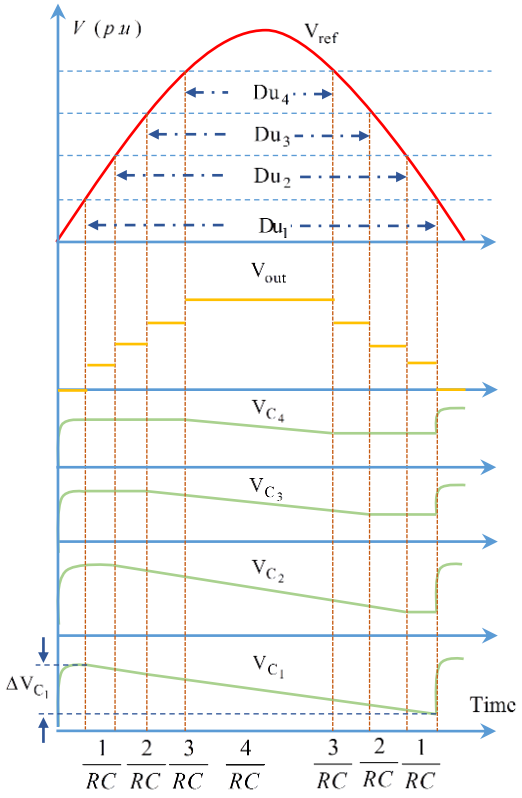
$$T_n=t_m-t_{m-1} \quad (8)$$

$$\begin{cases} m\in\{0,1,2,\ldots,(\ell-3)/2\} \\ n\in\{1,2,\ldots,(\ell-3)/2\} \\ b=(\ell-3)/2 \end{cases}$$

(a) (9) (b) (10) (c) (11) (d) (12)

(e) (13) (f) (14) (g) (15) (h) (16)

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TPEL.2018.2830401, IEEE Transactions on Power Electronics



(i)

Fig. 6. (a) to (h) voltage state in each level for a nine-level SCSS-CMI. (a), (b), (c), and (d) the zero, first, second, third, and forth levels in the rising side of the output voltage, respectively. (f), (g), and (h) the third, second, and first levels in the falling side of the output voltage, respectively.(i) voltage of each capacitor in different voltage-levels for a nine-level SCSS-CMI equipped with the first charging structure.

$$\Delta v_{c1} = \left(v_{dc} - v_{c1}(t_7)\right) Du_1 f / 2 \qquad (17)$$

$$\Delta v_{cn} = \left(v_{dc} - v_{cn}(t_{\ell-1-n})\right) Du_n f / 2 \qquad (18)$$

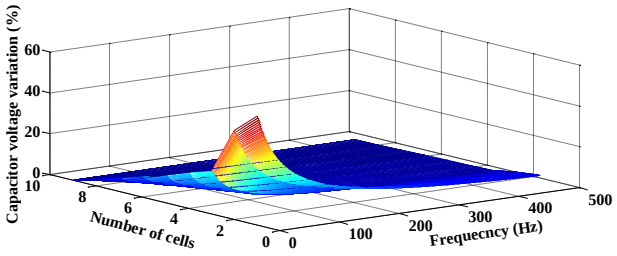


Fig. 7 Effects of the number of cells and frequency on the capacitors voltage drop

As mentioned earlier, the other factors which affects voltage in a SC cell are amount of the load current and power factor. To the end of analyzing the effects of these factors on the voltage, the schematic of SCSS-CMI, depicted in Fig. 8, is assumed. The symmetry of the output voltage shape will be guaranteed if the voltage values of the capacitors in the starting and ending of a half cycle become equal. Hence, the differences of voltage of the shown capacitor (v_{C_k}) in the starting and ending of a half cycle is considered as a criterion to evaluate the amount of dropped voltage in the capacitors. Equation (19) relates v_{C_k} for a half cycle. Also, equation (20) demonstrates initial value of v_{C_k} and (21) shows the same parameter at the end of the half cycle. The dropped voltage in C_k is asserted in (22). Fig. 9 visualizes the effects of the load current and angle (load power factor) on the capacitors voltage. In this evaluation, the capacitance of C_k and the output voltage frequency are, respectively 4700 μF, and 50 Hz. It is to be noted that, for the sake of clarity the effect of the changing process is not taken into account in this analyze, thus the actual voltage drop in a capacitor would be lower than the value which is figured out by equation (22). Equation (18) along with equation (22) can be used to figure out the voltage drop respect to the load, frequency, power factor, and capacitor size. Hence, in the designing stage these equations are useful to obtain the optimal size of the components respect to the admissible voltage drop of the H-bridge cells.

$$v_k(t) = v_{dc} + \frac{I_m}{c_k \omega}\cos(\omega t - \theta) \qquad (19)$$

$$v_k(0) = v_{dc} + \frac{I_m}{c_k \omega}\cos(\theta) \qquad (20)$$

$$v_k(\frac{\pi}{\omega}) = v_{dc} + \frac{I_m}{c_k \omega}\cos(\pi - \theta) = v_{dc} - \frac{I_m}{c_k \omega}\cos(\theta) \qquad (21)$$

$$\Delta v_k = v(0) - v(\frac{\pi}{\omega}) = \frac{I_m}{c_k \pi f}\cos(\theta) \qquad (22)$$

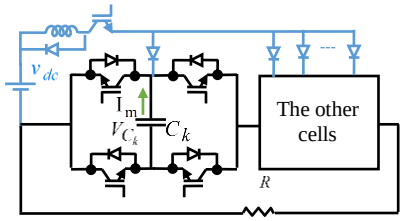


Fig. 8. Overall configuration of a typical SCSS-CMI.

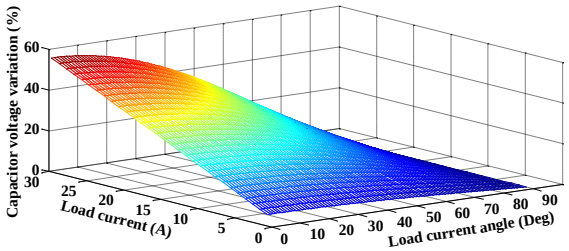


Fig. 9. Effects of load current and power factor on capacitors voltage drop.

IV. Simulation Results

In order to assess performances of the proposed topology it is tested under different conditions. To this end a nine-level SCSS-CMI is taken into consideration. The considered configuration is simulated under Mathlab/Simulink environment. The characteristics of the employed components are tabulated in Table IV.

TABLE IV
COMPONENTS CHARACTERISTIC

Component	value	unit
Input voltage (dc Voltage)	80	V
Charging inductor	6	mH
capacitors	4600	μF
Resistive load	1000	W
Resistive-Inductive load (0.6 lagging power factor)	1000	VA
Three-phase Resistive-Inductive load (0.8 lagging power factor)	3000	VA

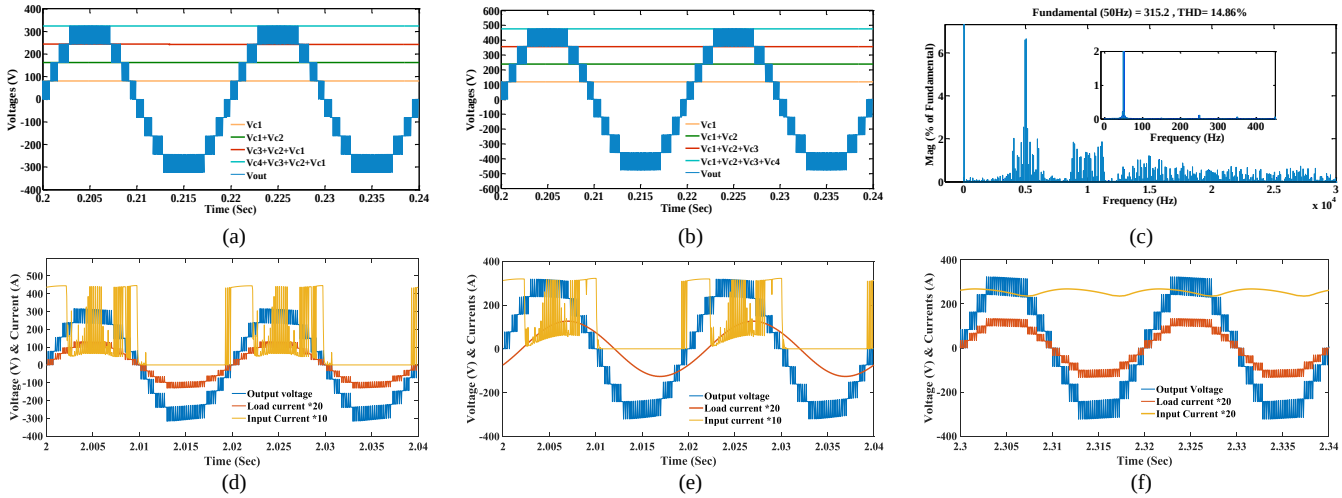
This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TPEL.2018.2830401, IEEE Transactions on Power Electronics

The desired voltage to be realized is a sinusoidal voltage with peak value of $220\sqrt{2}$ V (for modulation index of 1 (m=1)) and frequency of 50 Hz. Also level-shifted SPWM modulation strategy is considered to compute the switching signals. The simulated model is assumed to function under three different loading conditions. These three conditions are no-load condition, supplying a pure resistive load of 1000 W, and supplying a resistive-inductive load of 600 W with 0.6 lagging power factor. The output voltage along with the capacitors voltage under no load condition are shown in Fig. 10(a). For the sake of assessing the effect of the freewheeling diode, the output voltage and the capacitors voltage, under no-load condition and without using the freewheeling diode, are depicted in Fig. 10(b). Compared to the voltage shown in Fig. 10(a) it is evident that, in the case that the freewheeling diode is absent all the capacitors will be exposed to a perilous overcharging voltage of 120 V. This voltage is 40 V above the input dc voltage, so it can extremely damage the capacitors. Fig. 10(c) demonstrates the FFT analysis of the output voltage in no-load condition. Fig. 10(d), and (e) depict the output voltage, input current, and load current while the proposed inverter (equipped with the first charging structure) is feeding the pure resistive, and resistive-inductive loads, respectively. As the same, Fig. 10(f), and (g) show the output voltage, input current, and load current when the proposed inverter, equipped with the second charging structure, supplies the pure resistive, and resistive-inductive loads, respectively.

The other important parameter which needs a cautious inspection is charging currents of the capacitors. For the sake of inspecting this parameter, we assume that SCSS-CMI supplies the pure resistive load. Fig. 10(h), and (i) indicate the charging currents of the capacitors and the input charging currents when using the first, and second charging structures, respectively. According to these figures the spikes of the charging current are mitigated. So the capacitors are smoothly charged. Also comparing these figures it is understood that, the second charging structure offers a continuous and smoother input current. Therefore, in this structure the capacitors experience a charging current of lower magnitude in a longer time interval.

In order to assess the performance of SCSS-CMI in different modulation values, a varying modulation index is considered. The modulation index initially starts from 0.25, it changes to 0.98 at 1 sec., and at 3. sec., it falls to 0.68. Furthermore, different loading conditions are considered to provide a detailed investigation. Up to 3 sec., the load connected to the output terminal is considered to be a series R-L load of 10Ω+154mh (PF=0.2), at 2 sec., the load changes to a series connected R-L load of 58.4Ω+154mh, (PF=0.77). The load current, the output and capacitor voltages of SCSS-CMI equipped with the first, and second charging structures are respectively shown in Figs. 10(j), and (k). According to these figures, when the first charging structure is used the highest voltage fluctuation is 17 V (17/320*100=5.3%). However, using the second charging structure, the highest voltage fluctuation is 9 V. The reason is that, in the second charging structure the capacitors are charged during both the positive and negative half cycles. Moreover, these two figures prove the versatility of the proposed topology in different modulating indexes.

Furthermore, taking into consideration a nine-level three-phase configuration, the developed three-phase voltage, in the presence of a balanced resistive-inductive load, has been simulated. The three-phase output voltage together with the three-phase load current are shown in Fig. 10(l). The load for this three-phase configuration is considered to be a balanced load of 2400 W with 0.8 lagging power factor. Furthermore, in order to investigate the input current circumstance, a three-phase load of 3 kW (balanced pure resistive load) is considered. The input currents of the phases along with the total input current for the mentioned load are shown in Fig. 10(m). Moreover, in order to scrutinize the filter effect on the input current in the three-phase application, a LC-filter of ($L_f = 5$ mH and $C_f = 4700$ μF) is considered at the input side. Fig. 10(n) shows the input current when the considered three-phase SCSS-CMI supplies the mentioned 3 kW load. As shown, in the presence of the mentioned filter the three-phase SCSS-CMI imposes a continuous and smooth input current to the dc source. However, the filter slows down the dynamic behavior of the charging unit. It is to be noted that, since this work is not aimed at designing an optimal filter, the parameters of the filter are chosen indiscriminately, however, depending on the application, a more optimal filter could be designed to approach to a better performance.



This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TPEL.2018.2830401, IEEE Transactions on Power Electronics

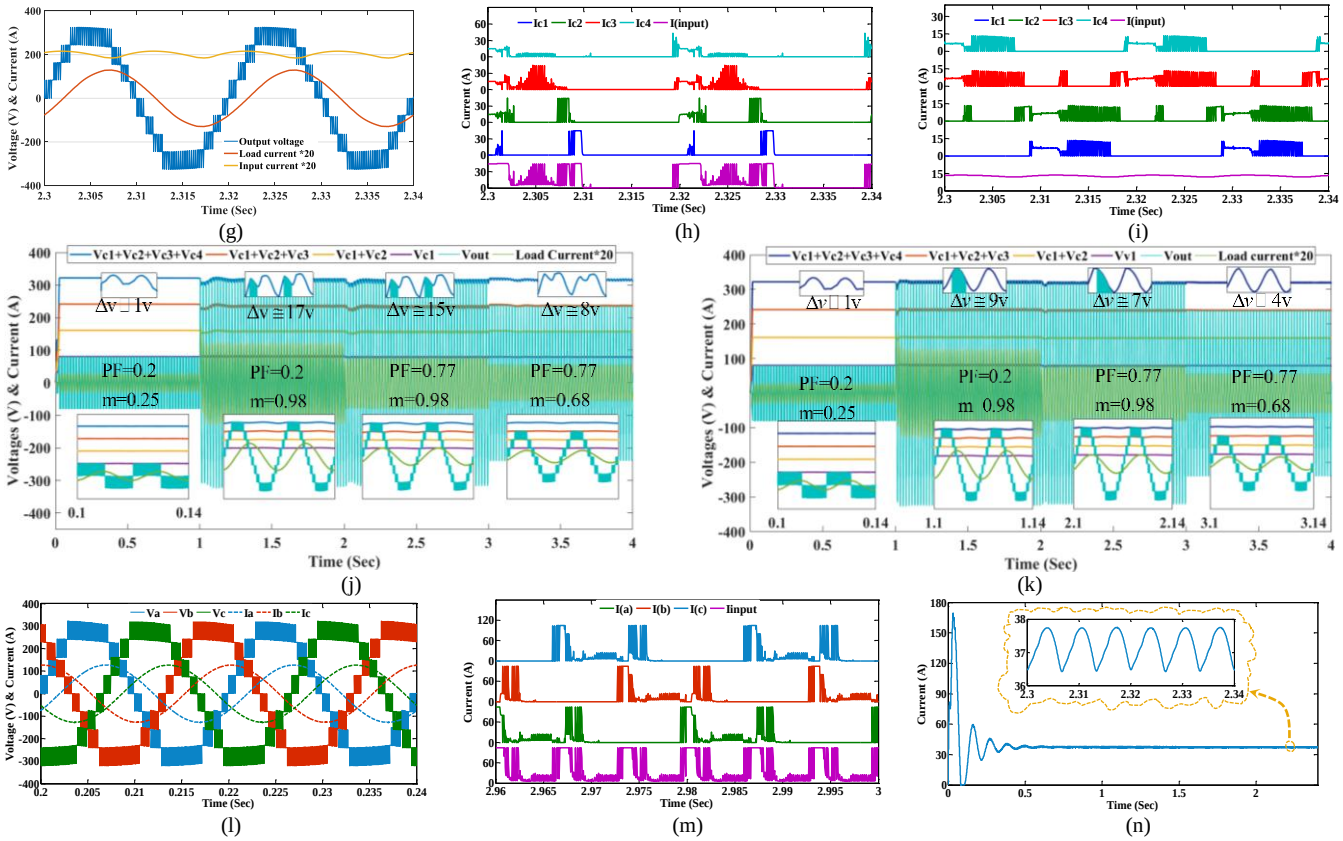


Fig. 10. (a) and (b), output and capacitors voltage under no-load condition with and without employing the freewheeling diode, respectively. (c) FFT analysis of the output voltage under no-load condition. (d) output voltage, load current, and input current under pure resistive loading condition (using the first charging structure). (e) output voltage, load current, and input current under resistive-inductive loading condition (using the first charging structure). (f) output voltage, load current, and input current under pure resistive loading condition (using the second charging structure). (g) output voltage, load current, and input current under resistive-inductive loading condition (using the second charging structure). (h), and (i) input and capacitors current when using the first and second charging structures, respectively. (j), and (k) load current, output and capacitors voltage with varying modulation index and PF, employing the first, and second charging structures, respectively. (l) load voltage and current of the three-phase SCSS-CMI. (m) total and phases input current in three-phase SCSS-CMI. (n) Input current in the presence of LC filter.

V. EXPERIMENTAL RESULTS

In order to lend credence to the feasibility of the suggested topology its performance is tested by employing a laboratory-built prototype. The specifications of the employed components along with the considered electrical values for the prototype, are listed in Table V. DSP-IDC28335Kv2 is adopted to compute the gates signals through LS-SPWM modulation strategy.

Since the two suggested charging structures have an identical CMI as the main part, they offer output voltages of identical characteristic. For this reason and for the sake of compactness only the output voltage developed by the first charging structure are shown in this section. However, because the suggested charging structures draw input currents of different characteristics, their input currents are investigated separately. Furthermore, in order to prove the extracted experimental results, in some cases the simulation results, which are obtained in the same condition as considered for the experimental tests, are also provided.

Firstly the output voltage under no-load condition is considered. The experimental result of the output voltage, under this condition, is depicted in Fig. 11(a). Since there is no-load, there appears no voltage drop at the output side. Fig. 11(b) shows the simulation result of the output voltage under the mentioned condition. For the sake of assessing the quality of the realized voltage the FFT analysis, taken by the experimental test, is shown in Fig. 11(c). As shown, since the switching frequency is 5 kHz, the dominant harmonics appear around multiples of this frequency. However, because this harmonics are significantly far from the fundamental frequency they can be easily eradicated by using a small filter.

The experimental, and simulation results of the output voltage together with the load current, under the condition of feeding a pure resistive load of 275 W, are, respectively, shown in Fig. 11(d) and (e). As shown, the active power brings about voltage drop to appear in the voltages of the capacitors, since the output voltage is combined with the voltages in the capacitors, voltage drops in the capacitors cause a total voltage drop to emerge at the output voltage. Since in the pure resistive load the voltages in the capacitors have the highest variation, this parameter is considered in Fig. 11(f). In this figure the ac component of the voltage in the capacitor which experiences the highest voltage variation, is depicted. Meantime the drawn current by the same capacitor is shown in Fig. 11(g). Moreover, to prove the capability of providing the reactive power, an inductive-resistive load of 275 W and 0.707 lagging power factor is employed. Fig. 11(h), and (i) show the experimental and simulation results of the output voltage and load current under inductive-resistive loading condition, respectively.

Since the dc unit (dc source and different charging structures) is only responsible for active power, the mentioned pure resistive loading condition is taken into consideration to scrutinize the input current circumstance at the presences of the suggested charging structures. Fig. 11(j) shows the input current when employing the first charging structure. As shown, the input current only flows in a half cycle and

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TPEL.2018.2830401, IEEE Transactions on Power Electronics

in the other half cycle it is zero. As noted earlier among the two structures the second structure stands out for its ability to draw a continuous and smooth current from the input side. Fig. 11(k) proves the mentioned feature of the second charging structure. The laboratory-built prototype is exhibited in Fig. 12.

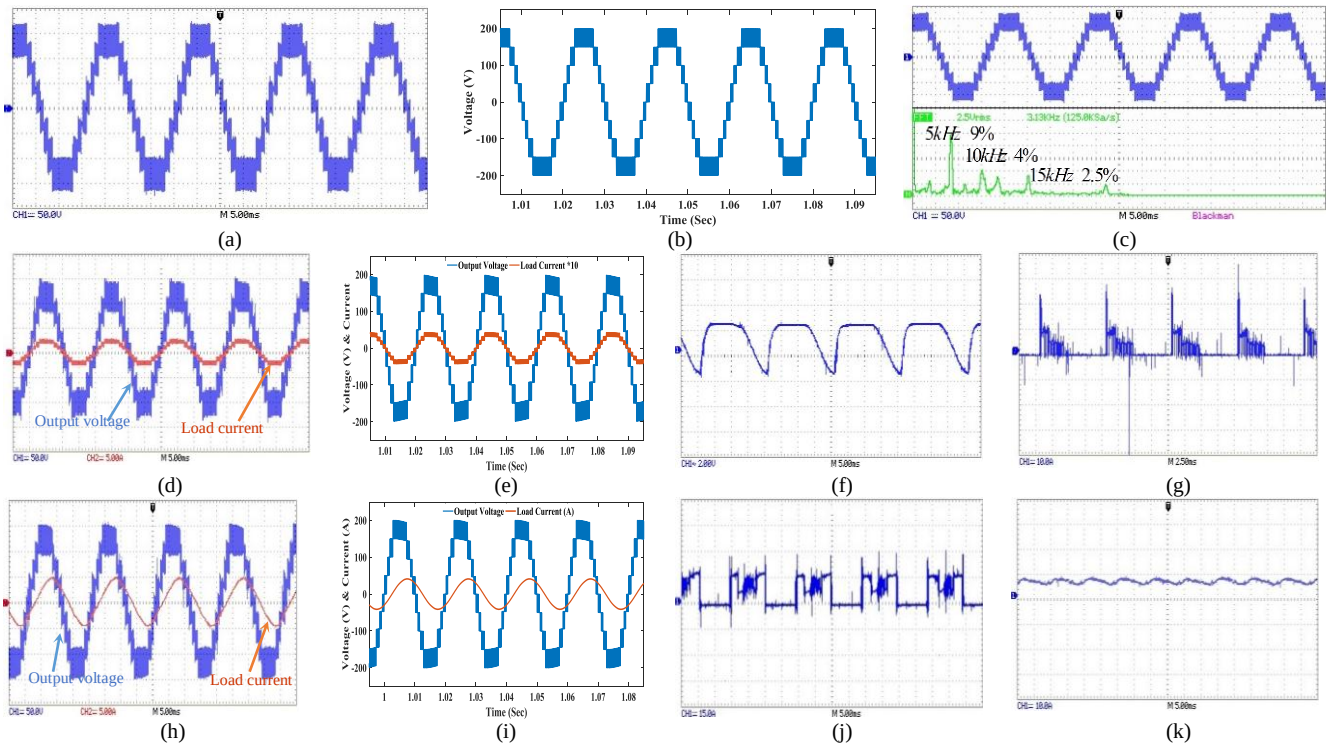


Fig. 11. (a), (b) experimental and simulation results of the output voltage under no-load condition, respectively. (c) FFT analysis of the output voltage. (d), and (e) Experimental and simulation results of the output voltage together with the load current under resistive loading condition, respectively. (f) Ac component of voltage in the capacitor experiencing the highest voltage variation. (g) The capacitor charging current. (h), and (i) Experimental and simulation results of the output voltage together with the load current under resistive-inductive loading condition, respectively. (j) Input current when employing the first charging structure. (k) Input current when employing the second charging structure.

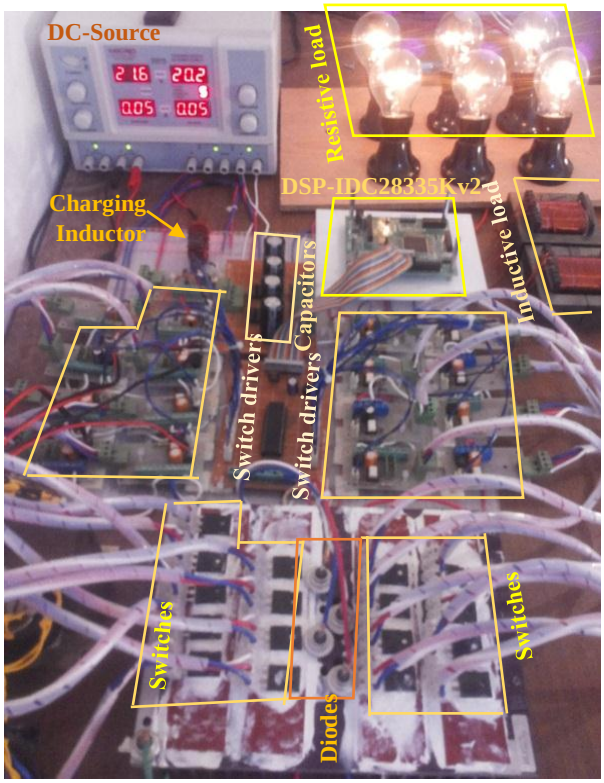


Fig. 12 Laboratory-built prototype SCSS-CMI

TABLE V
ELECTRICAL PARAMETERS AND COMPONENTS SPECIFICATIONS

Component	Specification	Electrical parameter	Value
Switches in main part	IRFP250	Pure resistive load	275 W (46.5 Ω)
Charging switch	IRFP460	Inductive-resistive load	389 VA (33 Ω +105 mH)
Opto-coupler	TLP250	rms valve of the output voltage	160
Capacitors	4700 μF	frequency of the output voltage	50 Hz
Charging inductor	6 mH	Input dc voltage	40 V
Diodes	Д242A	Switching frequency	5 kHz
		Number of H-bridges	4 (Nine-level)

VI. CONCLUSION

Although cascaded H-bridge multilevel inverter offers lots of advantages, it suffers from requiring several isolated dc sources. To the end of ridding this inverter of the mentioned drawback, this paper put forth a SC based CMI. In the proposed topology the dc sources have been replaced by some capacitors. Apart from using only one dc source, SCSS-CMI is able to offer a boosted staircase ac voltage. Since in the charging stages the employed capacitors could be exposed to some perilous inrush currents, a charging inductor is inserted along the charging current path to attenuate successive inrush currents. The charging inductor can limit the fault current as well. Meantime, a freewheel-

ing diode is connected to the charging inductor to avoid overcharge and stabilize the capacitors' voltage. Two different charging structures have been suggested. The main advantage of the first charging structure is offering a common ground for the dc and ac sides, which makes it a competent inverter for PV application, however it suffers from discontinuous input current. The second charging structure offers continuous input current but it losses the common ground feature. These structures along with a three-phase configuration have been thoroughly investigated in this work. Alike the single-phase configuration of SCSS-CMI a three-phase configuration requires only one dc source to charge all the capacitors of the phases, it features common ground feature as well as the first charging structure. By using a simulated model under Matlab/Simulink environment and a laboratory-built prototype the feasibility and viability of the suggested topology have been proven.

REFERENCES

[1] E. Villanueva, P. Correa, J. Rodriguez, and M. Pacas, "Control of a single-phase cascaded H-bridge multilevel inverter for grid-connected photovoltaic systems," *IEEE Trans. Ind. Electron.,* vol. 56, no. 11, pp. 4399-4406, Nov,2009

[2] A. K. Rathore, J. Holtz, T. Boller, "Generalized optimal pulsewidth modulation of multilevel inverters for low-switching-frequency control of medium-voltage high-power industrial ac drives," *IEEE Trans. Ind. Electron.,* vol. 60, no. 10, pp. 4215-4224, Oct. 2013.

[3] J. Pereda, J. Dixon, "23-level inverter for electric vehicles using a single battery pack and series active filters," *IEEE Trans. Veh. Technol.,* vol. 61, no. 3, pp. 1043 – 1051, Feb. 2012.

[4] M. Farhadi Kangarlu, E. Babaei, "A generalized cascaded multilevel inverter using series connection of submultilevel inverters," *IEEE Trans. Power Electron.*, vol. 28, no. 2, pp. 625-636, Feb. 2013.

[5] K. K. Gupta, A. Ranjan, P. Bhatnagar, L. K. Sahu, S. Jain, "multilevel inverter topologies with reduced device count: A review," *IEEE Trans. Power Electron.,* vol. 31, no. 1, pp. 135-151, Jan. 2016.

[6] H. Khoun Jahan, M. Naseri, M. M. Haji-Esmaeili, M. Abapour, K. Zare, "Low component merged cells cascaded-transformer multilevel inverter featuring an enhanced reliability," *IET Power Electron*., Vol. 10, no. 8, pp. 855-862, Jun. 2017.

[7] E. Samadaei, S. A. Gholamian, A. Sheikholeslami, J. Adabi, "An envelope type (E-Type) module: asymmetric multilevel inverters with reduced components," *IEEE Trans. Ind. Electron.,* vol. 63, no. 11, pp. 7148-7156, Nov. 2016.

[8] J. Rodriguez, J. Sheng Lai, F. Zheng Peng, "Multilevel inverters: a survey of topologies, controls, and applications," *IEEE Trans Ind. Electron.*, vol. 49, no. 4, pp.724-738, Aug. 2002.

[9] J. Rodriguez, S. Bernet, P. K. Steimer, I. E. Lizama, "A survey on neutral-point-clamped Inverters," IEEE Trans. Ind. Electron., vol. 57, no. 7, pp. 2219-2230, July 2010.

[10] M. Malinowski, K. Gopakumar, J. Rodriguez, M. A. Perez, "A survey on cascaded multilevel inverters," *IEEE Trans. Ind. Electron.*, vol. 57, no. 7, pp. 2197-2206, July 2010.

[11] B. Xiao, L. Hang, J. Mei, C. Riley, L. M. Tolbert, B. Ozpineci, "Modular cascaded H-bridge multilevel PV inverter with distributed MPPT for grid-connected applications," *IEEE Trans. Ind. Appl.*, Vol. 51, no. 2, pp. 1722-1731, Mar. 2015.

[12] L. K. Haw, M. S. A. Dahidah, H. A. F. Almurib, "A new reactive current reference algorithm for the STATCOM system based on cascaded multilevel inverters," *IEEE Trans. Power Electron.,* vol. 30, no. 7, pp. 3577-3588, July 2015.

[13] Y. Liu, A. Q. Huang, W. Song, S. Bhattacharya, G. Tan, "Small-signal model-based control strategy for balancing individual dc capacitor voltages in cascade multilevel inverter-based STATCOM," *IEEE Trans. Ind. Electron.* vol. 56, no. 6, pp. 2259-2269, June 2009.

[14] M. R. Banaei; H. Khounjahan, E. Salary. "Single-source cascaded transformers multilevel inverter with reduced number of switches," *IET Power Electron.* vol. 5, no. 9, pp. 1748-1753, Nov. 2012.

[15] S. G. Song, F. S. Kang, S. J. Park, "Cascaded multilevel inverter employing three-phase transformers and single dc input," *IEEE Trans. Ind. Electron*., vol. 56, no. 6, pp. 2005-2014, June 2009.

[16] J. Pereda, J. Dixon, "High-frequency link: A solution for using only one dc source in asymmetric cascaded multilevel inverters," *IEEE Trans. Ind. Electron*., vol. 58, no. 9, pp. 3884-3892, Sep. 2011.

[17] V. Sonti, S. Jain, S. Bhattacharya, "Analysis of the Modulation Strategy for the Minimization of the Leakage Current in the PV Grid-Connected Cascaded Multilevel Inverter," *IEEE Trans. on Power Electron.,* vol. 32, no. 2, pp.1156-1169, Feb. 2017.

[18] J. Fallah Ardashir, M. Sabahi, S. H. Hosseini, F. Blaabjerg, E. Babaei, G. B. Gharehpetian, "A single-phase transformerless inverter with charge pump circuit concept for grid-tied PV applications, " *IEEE Trans. Ind. Electron.*, vol 64, no. 7, pp. 5403 - 5415, Jul. 2017.

[19] W. Li, Y. Gu, H. Luo, W. Cui, X. He, and C. Xia, "Topology review and derivation methodology of single phase transformerless photovoltaic inverters for leakage current suppression," *IEEE Trans. Ind. Electron,.v*ol. 62, no. 7, pp. 4537–4551, July, 2015.

[20] Y. Gu, W. Li, Y. Zhao, B. Yang, C. Li, and X. He, "Transformerless inverter with virtual dc bus concept for cost-effective grid-connected PV power systems," IEEE Trans. Power Electron., vol. 28, no. 2, pp. 793-805, Feb. 2013.

[21] Yan Zhou, Hui Li, "Analysis and Suppression of Leakage Current in Cascaded-Multilevel-Inverter-Based PV Systems," *IEEE Trans. on Power Electron.,* vol. 51, no. 5, pp. 4212-4228, Oct. 2015.

[22] H. Khoun Jahan, F. Panahandeh, M. Abapour, S. Tohidi, "Reconfigurable Multilevel Inverter with Fault Tolerant Ability," IEEE Trans. on Power Electron. Vol. pp.1-1, no. 99, Nov. 2017.

[23] A. Ghazanfari, H. Mokhtari, M. Firouzi, "Simple voltage balancing approach for CHB multilevel inverter considering low harmonic content based on a hybrid optimal modulation strategy," *IEEE Trans. Power Delivery,* vol. 29, no. 10, pp. 5265-5277, Oct. 2014.

[24] A. Edpuganti, A. K. Rathore, "A survey of low-switching frequency modulation techniques for medium-voltage multilevel converters," *IEEE Trans. Ind. Appl*., vol. 51, no. 5, pp. 4212-4228, Oct. 2015.

[25] P. Udakhe, D. Atkar, S. Chiriki, V. B. Borghate, "Comparison of different types of SPWM techniques for three phase seven level cascaded H-Bridge inverter," *in proc, IEEE 1st International Conf. Power Electron., Intelligent Control and Energy Systems (ICPEICES)*.pp. 1-5, Jul. 2016.

[26] P. Sochor, H. Akagi, "Theoretical and experimental comparison between Phase-shifted PWM and level-shifted PWM in a modular multilevel SDBC inverter for utility-scale photovoltaic applications," *IEEE Trans. Ind. Appl.,* vol. 53, no. 99, pp. 1 – 1. May. 2017.